

## IN THE CLAIMS

What is claimed is:

- 1   **1.**    A mask identification circuit, comprising:  
2            a plurality of links arranged in series, each link having at least two  
3            inputs and at least two outputs, the inputs being directly coupled to the outputs  
4            in a first configuration, the inputs being cross coupled to the outputs in a  
5            second configuration.
- 1   **2.**    The mask identification circuit of claim 1, wherein:  
2            each link includes at least two conductive lines, the two conductive  
3            lines of a link having a first orientation in the first configuration and a second  
4            orientation in the second configuration.
- 1   **3.**    The mask identification circuit of claim 2, wherein:  
2            the two conductive lines of at least one link are parallel to one another  
3            in the first and second configuration.
- 1   **4.**    The mask identification circuit of claim 1, wherein:  
2            each link is formed on a different integrated circuit layer.

1 5. The mask identification circuit of claim 1, wherein:  
2 at least one link includes a first conductive line and a second  
3 conductive line, each conductive line having a downward contact to a link  
4 formed on a lower integrated circuit layer and an upward contact to a link  
5 formed on a higher integrated circuit layer.

1 6. The mask identification circuit of claim 5, wherein:  
2 the upward contacts are diagonal to one another.

1 7. The mask identification circuit of claim 1, wherein:  
2 the lower contacts are diagonal to one another.

1   **8.**     A mask identification code circuit, comprising:  
 2                 n mask identification (ID) bit circuits that each provide one bit of a  
 3                 mask identification code, where n is an integer greater than 1, and the mask ID  
 4                 bit circuits can provide more than n different mask identification codes.

1   **9.**     The mask identification code circuit of claim 8, wherein:  
 2                 each mask ID bit circuit includes a sense node that is coupled to one of  
 3                 at least two different potentials by at least two signal paths.

1   **10.**    The mask identification code circuit of claim 8, wherein:  
 2                 each mask ID bit circuit includes a sense node that is coupled to a first  
 3                 potential to identify one mask, to a second potential to identify a second mask  
 4                 and to the first potential to identify a third mask.

1   **11.**    The mask identification code circuit of claim 8, wherein:  
 2                 each mask ID bit circuit includes a plurality of separate signal paths  
 3                 cross coupled with one another to identify different masks.

1   **12.**    The mask identification code circuit of claim 8, wherein:  
 2                 each mask identification circuit includes a plurality of links, each link  
 3                 being formed on a different integrated circuit layer.

1     **13.**     The mask identification code circuit of claim 12, wherein:

2           each link of a mask identification circuit switches the potential  
3           supplied to the sense node when switched between configurations, each link  
4           including two conductive lines that are each coupled to a conductive line of  
5           another link by only one contact in both a first and second configuration.

1    **14.**    The mask identification code circuit of claim 8, wherein:

the mask ID bit circuits can provide  $2^n$  different mask identification codes with any combination of mask layer revisions.

1   **15.**   A method for identifying integrated circuit masks, comprising the steps of:  
2               forming mask bit identification (ID) circuits having interconnected  
3               links on a plurality of integrated circuit layers that provide a signal path to a  
4               sense node, each link being switchable between at least two configurations;  
5               and  
6               switching more than one link of a mask bit ID circuit from one  
7               configuration to another to represent multiple mask changes.

1   **16.**   The method of claim 15, wherein:  
2               forming interconnected links includes forming two conductive lines  
3               for each link, each conductive line having an upward contact and a downward  
4               contact, the upward contacts of the two conductive lines being essentially  
5               diagonal to one another, the downward contacts of the two conductive lines  
6               being essentially diagonal to one another.

1   **17.**   The method of claim 15, wherein:  
2               switching a link from one configuration to another includes changing  
3               the orientation of two conductive lines of the link.

1   **18.**   The method of claim 17, wherein:  
2               changing the orientation of the two conductive lines includes placing  
3               the two conductive lines essentially perpendicular to a previous orientation.

1   **19.**   The method of claim 15, wherein:  
 2               switching more than one link of a mask ID bit circuit includes  
 3               switching the configuration of one link for one mask change and switching the  
 4               configuration of a different link of the same mask ID bit circuit for another  
 5               mask change.

1   **20.**   The method of claim 15, wherein:  
 2               the links include one link comprising a polysilicon layer and another  
 3               link comprising an interconnect layer formed over the polysilicon layer.

